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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,566	09/22/2000	Takafumi Nakamura	197689US2	9678

22850 7590 11/29/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/667,566	NAKAMURA ET AL.
	Examiner	Art Unit
	Jeanne A. Di Grazio	2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *1-6 and 13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-12 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Priority to Japanese Patent Applications 11-271173 (Sept. 24, 1999) and 2000-281164 (Sept. 18, 2000) is claimed.

Drawings

The drawings were received on September 8, 2005. These drawings are Figures 1 and 2.

Claim Objections

Claim 7 (as amended) is objected to because of the following informalities:

Applicant recites "sources" in reference to switching elements.

'Sources' is not clear because sources may mean source electrodes or other features of the switching elements.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 7-12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) in view of United States Patent 5,668,650 (to Mori et al.).

As to claim 7 (amended), APA Figures 1 and 2 illustrate a conventional liquid crystal display having signal lines and scanning lines longitudinally and transversely arranged on an insulating substrate (Figure 1, and insulating substrate 1 and 4), a plurality of pixel electrodes (19) connected to respective intersections of said signal lines and said scanning lines via switching elements (not illustrated), a plurality of auxiliary capacity electrodes (3) electrically connected to said switching elements (not shown) and an auxiliary capacity feeder (6) disposed opposite to said auxiliary capacity electrode (3) via an insulating film (9).

APA does not appear to explicitly specify a first wiring layer connected to said auxiliary capacity electrode and a third wiring layer connected to an upper electrode connected to said pixel electrode and said switching elements and that the first wiring layer is formed on a layer closer to the lower side of the array substrate than the second wiring layer and the second wiring layer is formed on a layer closer to the upper side of the array substrate than the first wiring layer.

Mori teaches and discloses a thin film transistor panel having an extended source electrode in which (referring to Figure 2) a gate electrode (GE) and gate line (Lg) are connected to an auxiliary electrode (AG) and capacitance compensation electrode (CE)(Applicant's "a first wiring layer connected to said auxiliary capacity electrode"), a source and drain (SE and DE) connected to said switching elements (3) and gate electrode (Applicant's "a second wiring layer connected to said switching elements and said first wiring layer") and a third wiring layer (data line Ld). Furthermore, Mori shows that the gate electrode is on the lower side of the array substrate while the source, drain and switching elements are located towards the upper side of the array substrate (See Figure 2).

This configuration (as shown in Figure 2) results in total gate-source capacitance or sum of capacitance between facing portions of the gate electrode and source electrode and capacitance between facing portions of the auxiliary electrode and capacitance compensation electrode to be constant regardless of a variation in position of source electrode (Abstract, entire patent).

Mori claims that the elements are electrically connected to each other (See, for example Mori claim 1).

Mori is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion and motivation to include a first wiring layer connected to said auxiliary capacity electrode and a third wiring layer connected to an upper electrode connected to said pixel electrode and said switching elements and that the first wiring layer is formed on a layer closer to the lower side of the array substrate than the second wiring layer and the second wiring layer is formed on a layer closer to the upper side of the array substrate than the first wiring layer for constant capacitance regardless of the position of the source electrode.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify APA in view of Mori to cancel a change in gate-source capacitance due to alignment error and for the other above noted reasons (Abstract, entire patent).

As to claim 8, the source / drain and switching elements are not superimposed upon the capacitance compensation electrode (Figure 2).

As to claim 9, the gate electrode is formed on the same layer as the auxiliary electrode (Figure 2).

As to claim 10, source / drain / switching elements and data lines are presumed to be formed on a same layer as an upper electrode.

As to claim 11, the length of the gate electrode is presumed to be equal to that of source / drain switching elements.

As to claim 12, Mori teaches and discloses the use of I and n type semiconductor films).

As to claim 17, the switching elements in clued gate, drain and source electrodes and drain and data lines are connected to the switching elements (Figure 2).

Response to Arguments

Applicant's arguments filed 8 September 2005 have been fully considered but they are not persuasive.

Applicant argues a lack of electrical connection among the various recited wiring layers.

However, as best understood by the Examiner, and as claimed in Mori, the various structures are electrically connected. See, for example, Mori claim 1.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio
Patent Examiner
Art Unit 2871

JDG

ANDREW SCHECHTER
PRIMARY EXAMINER